UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,611	03/31/2000	Carl M. Ellison	042390.P8112	2172

8791 7590 08/26/2004

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TRAN, ELLEN C	

ART UNIT	PAPER NUMBER
2134	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,611	ELLISON ET AL.	
	Examiner	Art Unit	
	Ellen C Tran	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Jan-Jul 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communication: amendment filed on 07 May 2004, with an original filing date of 31 March 2000.

2. Claims 1-60 are currently pending in this application. Claims 1, 16, 31, and 46 are independent claims.

3. Applicant's amendment is accepted.

Response to Arguments

4. Applicant's arguments with respect to claims 1-60 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language

6. **Claims 1-60** are rejected under 35 U.S.C. 102(e) as being anticipated by Carloganu et al. U.S. Patent No. 6,226,749 (hereinafter '749).

As to independent claim 16, "A method comprising: configuring an access transaction generated by a processor by a configuration storage containing configuration parameters, the processor having a normal execution mode and an

isolated execution mode, the access transaction having access information; and" is taught in '749 col. 3, lines 30-59;

"checking the access transaction by an access checking circuit using at least one of the configuration parameters and the access information" is shown in '749 col. 4, lines 44-63.

As to dependent claim 17, "wherein the configuration parameters include an isolated setting and an execution mode word" is disclosed in '749 col. 5, lines 1-30.

As to dependent claim 18, "wherein the access information comprises a physical address and an access type, the access type indicating if the access transaction is one of a memory access, an input/output access, and a logical processor access, the physical address being one of a translation lookaside buffer (TLB) physical address from a TLB and a front side bus (FSB) physical address from an FSB" is taught in '749 col. 4, lines 44-67 and col. 9, lines 57-67.

As to dependent claim 19, "wherein configuring the access transaction comprises: defining an isolated memory area corresponding to a memory external to the processor by the isolated setting contained in a setting storage" is shown in col. 20, line 55 through col. 21, line 45.

As to dependent claim 20, "wherein defining the isolated memory area comprises: forming the isolated setting by a combination of at least two of a base value, a mask value, and a length value stored in a base register, a mask register, and a length register, respectively" is disclosed in '749 col. 8, lines 34-67.

As to dependent claim 21, "wherein configuring the access transaction further comprises: asserting the execution mode word stored in a processor control register when the processor is configured in the isolated execution mode" is taught in '749 col. 2, lines 42-49.

As to dependent claim 22, "wherein checking the access transaction comprises: detecting if the TLB and FSB physical addresses are within the isolated memory area defined by the isolated setting by TLB and FSB address detectors, respectively, the TLB and FSB address detectors generating processor and FSB isolated access signals, respectively" is shown in '749 col. 9, lines 40-67.

As to dependent claim 23, "wherein checking the access transaction further comprises: generating a processor snoop access signal by a snoop checking circuit" is disclosed in '749 col. 7, lines 43-60.

As to dependent claim 24, "wherein generating the processor snoop access signal comprises: combining a cache access signal, the FSB isolated access signal, and an external isolated access signal from another processor by a snoop combiner, the combined cache access signal, the processor isolated access signal and the external isolated access signal corresponding to the processor snoop access signal" is taught in '749 col. 9, lines 40-67.

As to dependent claim 25, "wherein checking the access transaction further comprises: generating an access grant signal indicating if the access transaction is valid by an access grant generator" is shown in '749 col. 9, lines 20-39.

As to dependent claim 26, "wherein the logical processor access is one of a logical processor entry and a logical processor exit" is disclosed in '749 col. 7, lines 40-61.

As to dependent claim 27, "wherein checking the access transaction comprises: managing a logical processor operation caused by the logical processor access by a logical processor manager" is taught in '749 col. 7, lines 33-42.

As to dependent claim 28, "wherein managing the logical processor operation comprises: storing a logical processor count indicating a number of logical processors currently enabled in a logical processor register; enabling a logical processor state when the logical processor access is valid by a logical processor state enabler; updating the logical processor count according to the logical processor access by a logical processor updater, the logical processor updater being enabled by the enabled logical processor state; determining if the logical processor count is equal to a minimum logical processor value by a minimum detector; and determining if the logical processor count exceeds a maximum logical processor value by a maximum detector" is shown in '749 col. 1, lines 40-48.

As to dependent claim 29, "wherein updating the logical processor count comprises: initializing the logical processor register when there is no enabled logical processor" is disclosed in '749 col. 8, lines10-20.

As to dependent claim 30, "wherein updating the logical processor count comprises: updating the logical processor count in a first direction when the access transaction corresponds to the logical processor entry; and updating the logical processor count in a second direction opposite to the first direction when the access transaction corresponds to the logical processor exit" is taught in '749 col. 9, lines 20-56.

As to independent claims 1, this claim is the apparatus comprising the same method of claim 16 and is similarly rejected along the same rationale.

As to independent claim 31, this claim is a chipset comprising the same method as claim 16 and is similarly rejected along the same rationale.

As to independent claim 46, this claim is a computer program product comprising the same method as claim 16 and is similarly rejected along the same rationale.

As to dependent claims 2-15, 32-45, and 47-60 these claims incorporated substantially similar subject matter as cited in claims 17-31 above and are similarly rejected along the same rationale.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ellen C Tran whose telephone number is (703) 305-8917. "**After mid-Oct, 2004, the examiner can be reach at (571) 272-3842".** The examiner can normally be reached on 6:30 am to 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A Morse can be reached on (703) 308-4789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ellen. Tran
Patent Examiner
Technology Center 2134
30 July 2004

GREGORY MORSE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100